QPLL User Manual

Quartz Crystal Based Phase-Locked Loop for Jitter Filtering Application in LHC

Paulo Moreira

CERN - EP/MIC, Geneva Switzerland

2002-12-10

Version 0.0

Technical inquires: Paulo.Moreira@cern.ch

Preliminary

Introduction 3

Features: 3

OPERATION 4

QPLL Signals 5

QPLL pinout 7

Pin assignments 7

INTRODUCTION

The QPLL is a Quartz crystal based Phase-Locked Loop. Its function is to act as a jitter-filter for clock signals operating synchronously with the LHC bunch crossing clock frequency. Two frequency multiplication modes are implemented: 120 MHz and 160 MHz modes[1]. In the 160 MHz mode, the ASIC generates three clock signals synchronous with the reference clock at 40 MHz, 80 MHz and 160 MHz while in the 120 MHz mode the synthesized frequencies are 40 MHz, 60 MHz and 120 MHz. In both cases, the highest frequency is generated directly from a Voltage Controlled Crystal Oscillator (VCXO) and the lower frequencies are obtained by synchronous division. The two frequency multiplication modes require Quartz crystals cut to the appropriate frequencies.

Features:

- Quartz crystal based Phase-Locked Loop
- Three LVDS clock outputs
- Two frequency multiplication modes:
  - 40 MHz, 80 MHz and 160 MHz
  - 40 MHz, 60 MHz and 120 MHz
- Reference clock input levels:
  - LVDS
  - CMOS single-ended, 2.5 V to 5 V compatible
- Output jitter: < 50 ps peak-to-peak for input signal jitter less than 120 ps RMS
- Package: LPCC-28 (5 mm × 5 mm, 0.5 mm pitch)
- Power supply voltage: 2.5V
- Radiation tolerant
- 0.25 μm CMOS technology
- Crystal: The QPLL quartz crystal will be provided with the QPLL for operation in the specified frequency multiplication mode.

[1] Please note that frequency numbers in this document are often rounded to the nearest integer. This is just a simplification to facilitate reading (and writing). In fact, these numbers should be interpreted to be the exact multiples of the LHC bunch-crossing clock frequency.

OPERATION

The QPLL uses the LHC bunch-crossing clock as the reference frequency. This signal can be feed to the ASIC either in CMOS or LVDS levels (please refer to Figure 1). Selection of which input to use is simply done by forcing the unused clock input to logic level “0” (notice the use of the OR function in the reference clock signal path in the block diagram). The three clock outputs are LVDS signals and their frequency depends on the “*mode*” input. When “*mode*” is set to “0” the output clock frequencies are: 40 MHz, 60 MHz and 120 MHz otherwise the frequencies are: 40 MHz, 80 MHz and 160 MHz. Since the highest clock frequency is obtained directly from the Voltage Controlled Crystal Oscillator (VCXO), different crystals are required for operation in each one of the two frequency multiplication modes. The required crystals are provided by CERN for the specified operation frequency.

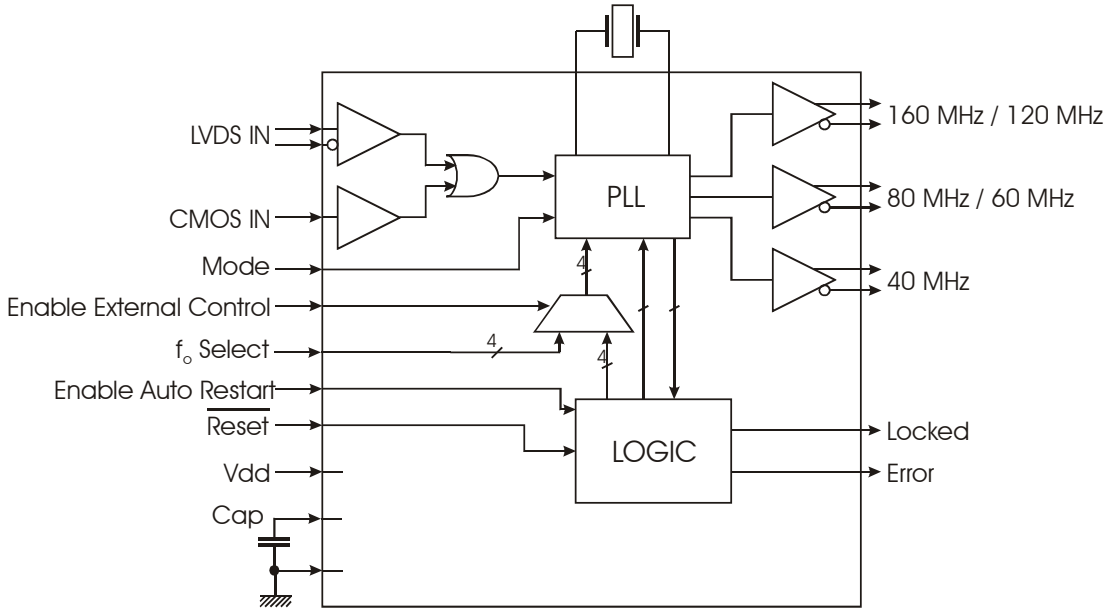

Figure 1 QPLL block diagram

The use of a VCXO in the QPLL allows to achieve low jitter figures but imposes the limitation of a small frequency lock range. To cope with crystal cutting accuracy, process, temperature and power supply variations, upon reset or loss of lock, the ASIC goes through a frequency calibration procedure. In principle, this is an automatic procedure that in most applications should be “transparent” to the user. However in some situations, like for example hardware or system testing, the user might want to have control over it. The signals that are relevant to this function are: “*externalControl*”, “*autoRestart*” and “*f_oSelect<3:0>*”. If the “*externalControl*” signal is set to “1” then the automatic calibration procedure is disabled and the VCXO centre frequency is set by the signals “*f_oSelect<3:0>*” otherwise, the free running frequency is automatically determined.

The QPLL contains a lock detection circuit that monitors at every instant the lock state of the phase-locked loop. If the PLL is detected to be unlocked, a frequency calibration cycle is initiated to lock the PLL. This feature can be disabled by forcing the signal “*autoRestart*” to “0”. In this case, a frequency calibration cycle is only started if a reset is applied to the IC. In any case the “*locked*” signal reports the locked status of the PLL.

The logic circuits controlling the PLL use redundant logic techniques to cope with Single Event Upsets (SEU). The “error” flag indicates (momentarily) that one SEU has occurred. These errors are dealt with automatic requiring no action from the user.

QPLL SIGNALS

autoRestart – 5V compatible CMOS input with internal pull-up resistor:

autoRestart = "0": Automatic restart of the PLL is disabled. A frequency calibration cycle will only occur after a reset.

autoRestart = "1": Automatic restart is enabled. A frequency calibration cycle will occur each time the PLL is detected to be unlocked.

cap – VCXO decoupling node:

A 100 nF capacitor must be connected between this pin and ground.

error – 2.5V CMOS output:

This signal indicates that an SEU has occurred. Since SEU events are dealt with automatically by the ASIC logic, this signal will be active only during period in which the error condition persists. A SEU should not affect the operation of the PLL

externalControl – 5V compatible CMOS input with internal pull-down resistor:

externalControl = "0": The VCXO centre frequency is set by the automatic frequency calibration procedure.

externalControl = "1": The VCXO free running frequency is set by the input signals f_o*Select<3:0>.*

f_oSelect<3:0> - 5V compatible CMOS inputs with internal pull-down/pull-up resistors (f_o*Select<3>* ← pull-up, f_o*Select<2>* ← pull-down, f_o*Select<1>* ← pull-down, f_o*Select<0>* ← pull-down):

These signals control the VCXO free running oscillation frequency when the signal "*externalControl*" is set to "1". If "*externalControl*" is set to "0" these signals have no influence on the IC operation.

inCMOS – 5V compatible CMOS input with internal pull-down resistor:

This is the CMOS reference clock input. When in use, *inLVDS+* and *inLVDS-* must be set to logic levels "0" and "1" respectively.

inLVDS+ and inLVDS- – LVDS inputs:

These signals are the LVDS reference clock inputs. When in use, *inCMOS* must be held at logic level "0".

locked – 2.5V CMOS output:

Reports the PLL locked status.

Lvds40MHz+ lvds40MHz- – LVDS output:

40MHz clock output

lvds80MHz+ lvds80MHz- – LVDS output:

mode = "0": 60 MHz clock signal (with 120 MHz quartz crystal).

mode = "1": 80 MHz clock signal (with 160 MHz quartz crystal).

lvds160MHz+ lvds160MHz- – LVDS output.

mode = "0": 120 MHz clock signal (with 120 MHz quartz crystal).

mode = "1": 160 MHz clock (with 160 MHz quartz crystal).

mode – 5V compatible CMOS input with internal pull-up resistor:

mode = "0": 120 MHz frequency multiplication mode (120 MHz quartz crystal required).

mode = "1": 160 MHz frequency multiplication mode (160 MHz quartz crystal required).

~reset – 5V compatible CMOS input:

Active low reset signal.

xtal1, xtal2 – Quartz crystal connections

QPLL PINOUT

The QPLL is packaged in a 28-pin 5 mm × 5 mm Leadless Plastic Chip Carrier (LPCC-28) with 0.5 mm pin pitch.

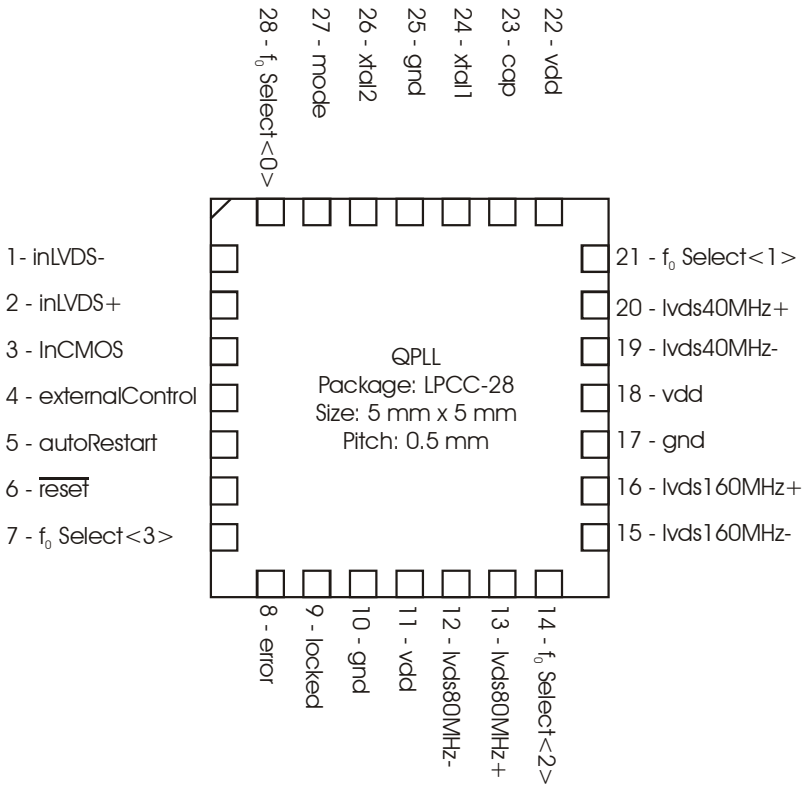

Figure 2 QPLL pinout

Pin assignments

Pin Number	Signal Name	Signal type
1	inLVDS-	Input, LVDS
2	inLVDS+	Input, LVDS
3	inCMOS	Input, CMOS 5V compatible
4	externalControl	Input, CMOS 5V compatible
5	autoRestart	Input, CMOS 5V compatible
6	~reset	Input, CMOS 5V compatible
7	f_0Select<3>	Input, CMOS 5V compatible
8	error	Output, 2.5 V compatible
9	locked	Output, CMOS 2.5 V
10	gnd	Power
11	vdd	Power

12	lvds80MHz-	Output, LVDS
13	lvds80MHz+	Output, LVDS
14	f_0Select<2>	Input, CMOS 5V compatible
15	lvds160MHz-	Output, LVDS
16	lvds160MHz+	Output, LVDS
17	gnd	Power
18	vdd	Power
19	lvds40MHz-	Output, LVDS
20	lvds40MHz+	Output, LVDS
21	f_0Select<1>	Input, CMOS 5V compatible
22	vdd	Power
23	cap	Power
24	xtal1	Analogue, Quartz crystal
25	gnd	power
26	xtal2	Analogue, Quartz crystal
27	mode	Input, CMOS 5V compatible
28	f_0Select<1>	Input, CMOS 5V compatible